

Blue Pearl Software 사 Clock Domain Crossing

A. 목적 : Analysis for CDC metastability

B. 구분 : Advanced multi-clocking techniques for high-performance and low-power requirements

C. Supported Platform and O/S System

- RHEL 6, 7, 8 (64 bit)
- Windows 7, 8.1, 10 (64 bit)

D. 특성 및 기능

- Analyze RTL 이후 진행 가능한 Option Feature
- Synchronized / Unsynchronized Device에 대한 Global Standard 기반 Clock Tree 분석
- Transitive/Non-Transitive Clock Domain Grouping을 통해 Clock Tree를 단순 도식화 (Advanced Clock Env.)
- RTL Code 및 Schematic에 대한 Cross-probing을 활용한 Clock 분석
- User Grey Cell (UGC)을 이용한 Black box Design에 대한 Boundary Clock 분석 가능

Advanced Clock Environment File
Total number of Clock Domains: 2 Total number of Clocks: 9
Clock Domains:

From	To	# Synchronized	# Unsynchronized	Derived?	Equivalent?
clk	ip1_inst.clk_d2	0	0	Yes	No
clk3	clk4	1	4	No	No
clk4	clk5	1	2	No	No

DFFs/Output Port CDC Crossings:

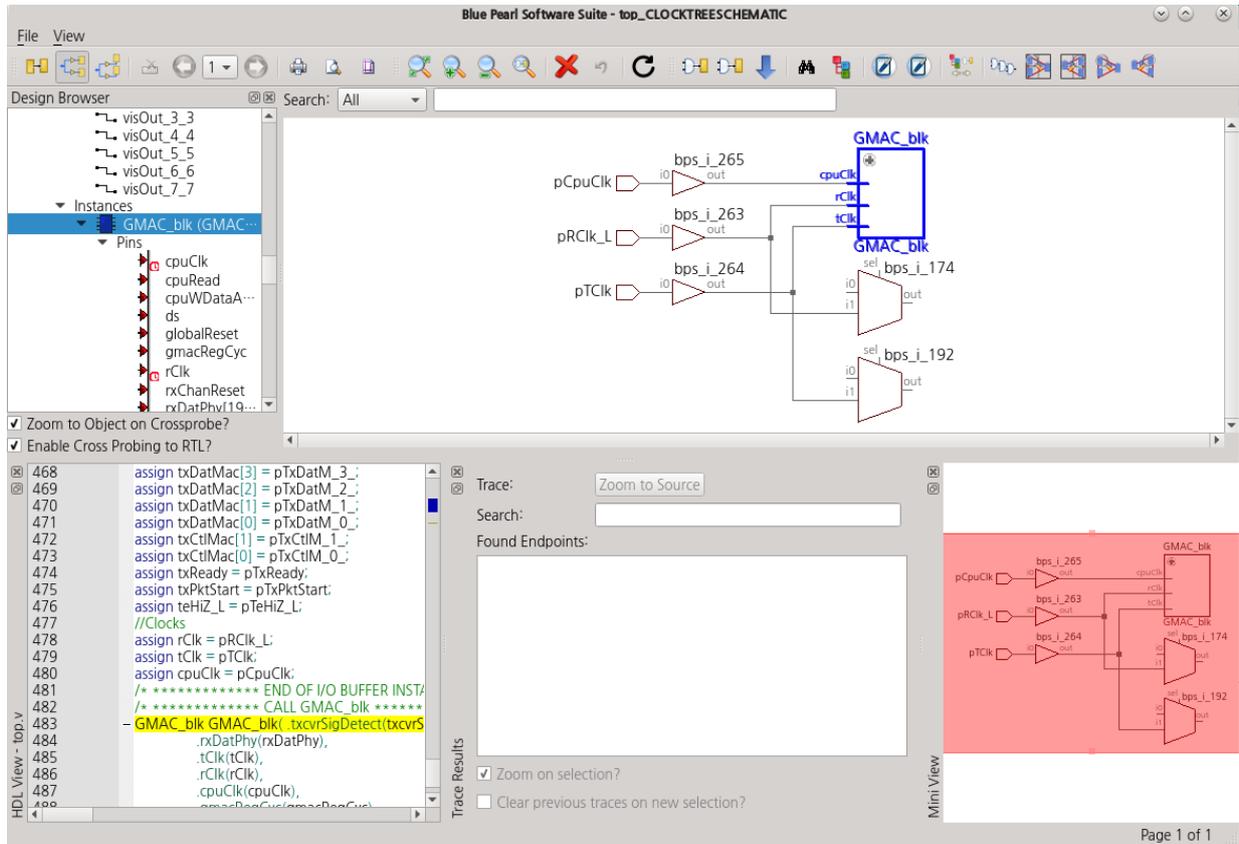
DFF Name	Synchronized?
tc.ip9_insta.sync1	Yes
tc.ip4_inst.qcdc1	No
tc.ipa_instc.qcdc1	No

```

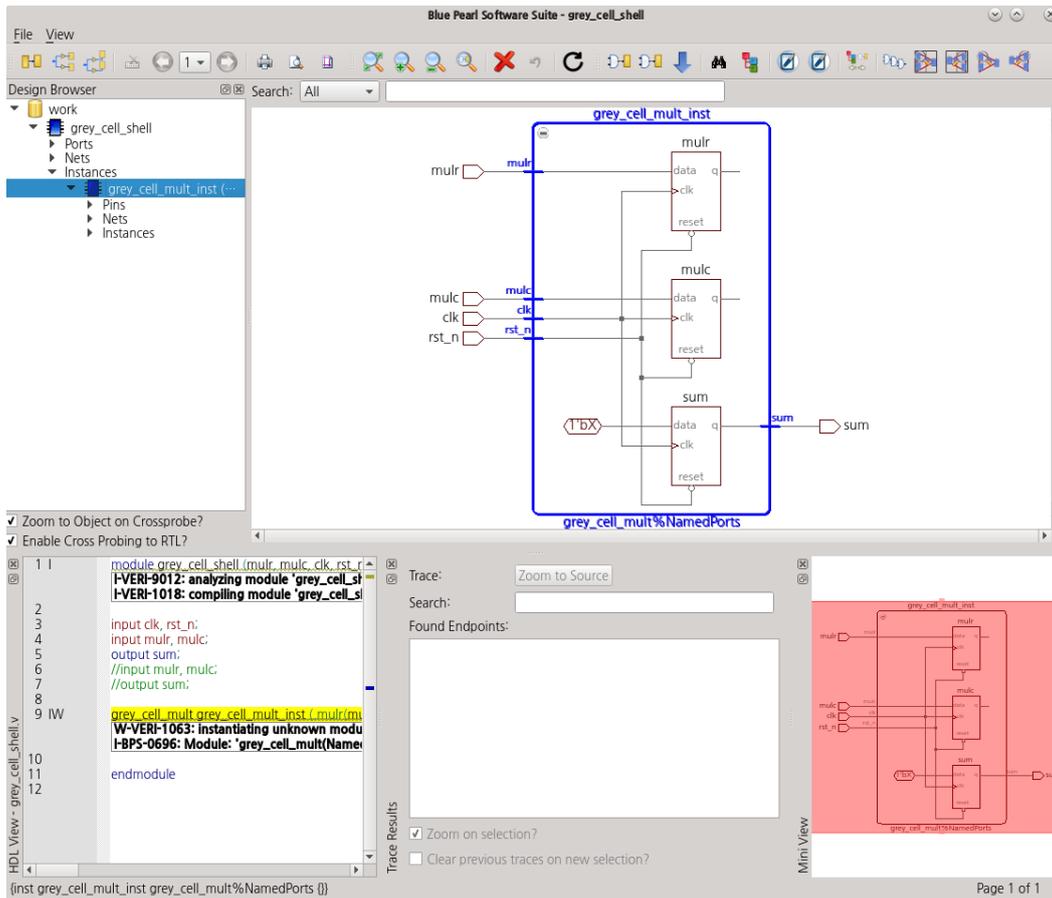
214     sync2 <= '1'b0;
215   end
216   else
217     begin
218       sync1 <= in ;
219       sync2 <= sync1 ;
220     end
221   end
222 end
223 endmodule
224
  
```

Clock Interaction From: clk_group.clk3 To: clk_group.clk4

Clock Domain Grouping 을 통해 간편한 Clock Tree 확인



Clk Pin 에 한정한 RTL Code 와 Schematic 간 Cross-probing 기능 활용 지원



User Grey Cell 을 이용한 Black Box Design 분석 가능

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